POWERMASTER SEMICONDUCTOR

Masters of Power Solution

Comparative Analysis of SiC MOSFETs and Super-Junction MOSFETs: Key Differences and Performance Implications

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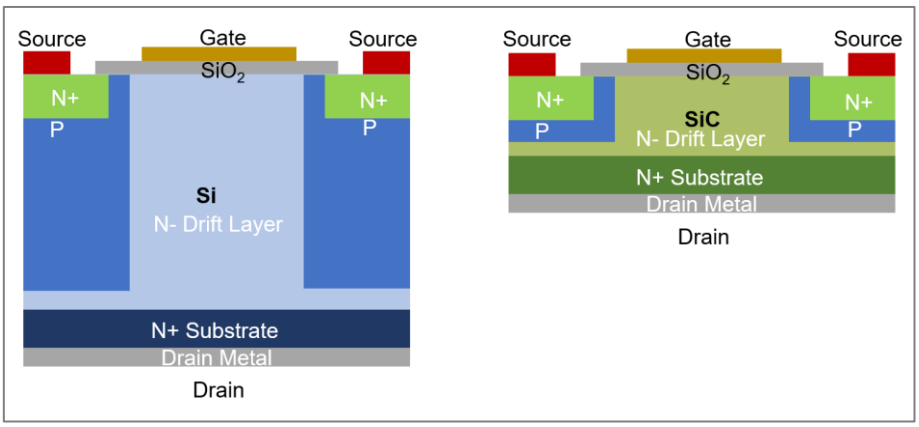
1. Introduction

In the voltage range of 500~900V, Super-junction MOSFETs are widely used in various applications such as server and telecommunication power supplies, on-board chargers (OBC) and energy storage systems (ESS). Recently, 650~750V SiC MOSFETs have been quickly gaining adoption, particularly in bridge-type topologies due to their superior characteristics that enable higher power density, improved system efficiency and the fulfillment of bi-directional operation requirements.[1]~[2]. This application note will explore a comparative analysis of key parameters between SiC MOSFET and Super-junction MOSFET and how each characteristic affects different topologies.

2. SiC MOSFET vs. Si Super-Junction MOSFET

2.1.1. On-Resistance Characteristics vs. Temperature

While MOSFET technologies and cell structures have dramatically changed through the years, the vertical cell structure of a MOSFET has been optimized to reduce $R_{DS(ON)}$ in the same die size while improving Figures of Merit (FOM) such as $R_{DS(ON)} \times Q_G$, $R_{DS(ON)} \times E_{OSS}$ and $R_{DS(ON)} \times Q_{OSS}$. In high-voltage MOSFET technologies, the most remarkable achievement for on-resistance reduction is Super-junction technology. As shown in Fig. 1 (a), Super-junction technology has a deep p-type pillar-like structure in the body in contrast to the well-like structure of conventional planar technology to reduce drift resistance. As a result, Super-junction MOSFETs have become the mainstream for high-performance Si MOSFETs in the voltage range of 500~900V. Essentially, the SiC material has a significantly higher critical breakdown voltage than Si, enabling a thinner drift layer and higher doping concentration in the drift layer region, as shown in Fig. 1.



(a) Super-Junction MOSFET (b) SiC MOSFET

Figure 1. Vertical Structure of Power MOSFET

Consequently, this results in a drastic reduction in on-resistance ($R_{DS(ON)}$) for a given die size and voltage rating, contributing to greater efficiency by minimizing power losses. $R_{DS(ON)}$ is determined by the sum of the resistances from the drain to the source which includes the resistance of the SiC substrate (R_{SUB}), the epitaxial layer resistance of the drift layer (R_{DR}), the resistance of the junction field-effect transistor, JFET (R_{JFET}), channel resistance (R_{CH}) and source contact resistance (R_S) as well as wire bonding and lead frame resistances. As shown in Fig. 2, the percentage of resistance associated with each region varies dramatically depending on the material and technology used at the same voltage rating. The major contribution to $R_{DS(ON)}$ in high-voltage Si MOSFETs is the epitaxial layer resistance of the drift layer. Unlike Si MOSFETs, where the drift layer plays a significant role, the channel resistance is dominant in $R_{DS(ON)}$ for SiC MOSFETs.

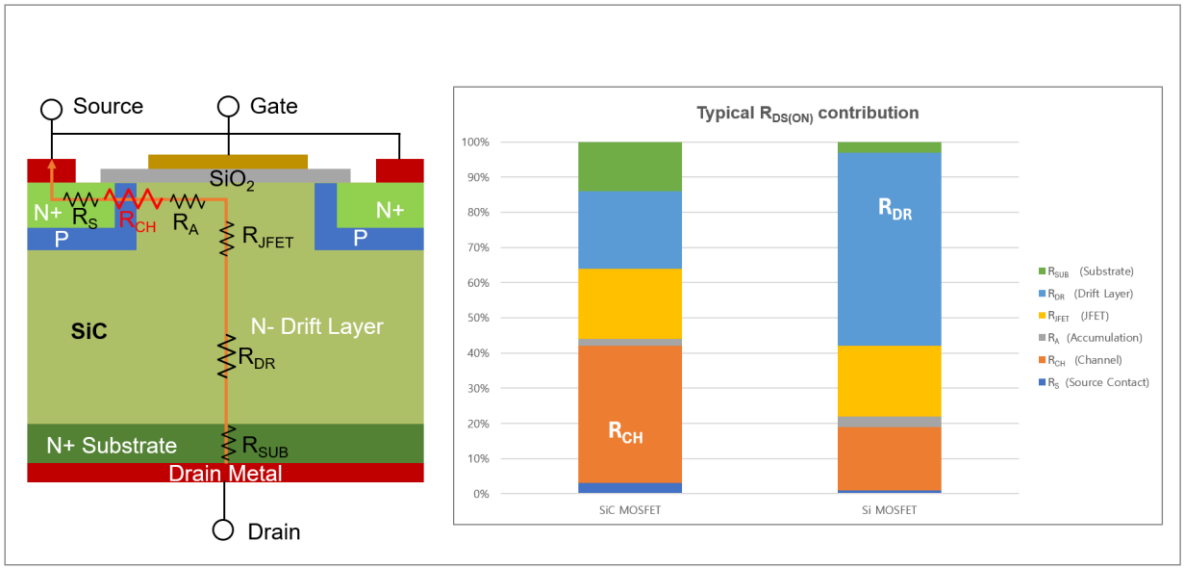


Figure 2. Relative Contribution to $R_{DS(ON)}$ of 650V Different Technologies: SiC MOSFET vs Si MOSFET

The drain-source on-resistance, $R_{DS(on)}$ is one of the key parameters of a MOSFET. In the datasheet, both typical and maximum ratings at 25°C are specified. MOSFET on-resistance exhibits PTC (Positive Temperature Coefficient) characteristics, indicating that the on-resistance increases at higher temperatures. Thanks to the PTC characteristics of MOSFET, it is generally easier to operate parallel MOSFETs due to self-stabilization. At high temperatures, the on-resistance of Super-junction MOSFETs significantly increases due to the high proportion of epitaxial drift layer resistance in the overall on-resistance. Although the epitaxial drift layer resistance of SiC MOSFETs also exhibits a similar temperature dependency to Super-junction MOSFETs, the rate of increase in the overall on-resistance of SiC MOSFETs is much lower than that of Super-junction MOSFETs because of the small proportion of epitaxial drift layer resistance in the overall on-resistance, as shown in Fig. 3. As shown in Tabe 1, SiC MOSFETs show much lower temperature dependency of $R_{DS(ON)}$ than Super-junction MOSFET. The multiplication factor from 25°C to 100°C and from 25°C to 175°C for $R_{DS(ON)}$ is 1.15 and 1.45 for SiC MOSFETs, and 1.65 and 2.64 for Super-junction MOSFETs, respectively. This means that a higher $R_{DS(ON)}$ SiC MOSFET can replace a lower $R_{DS(ON)}$ Super-junction MOSFET with same conduction loss and lower switching losses in applications.

Table 1. Temperature dependency of the $R_{DS(ON)}$ SiC MOSFET vs. Super-junction MOSFET

$R_{DS(ON)}$ @ V_{GS}=18V	SiC MOSFET	Super-junction MOSFET
$R_{DS(ON)}$ Temp. coefficient (100°C/25°C) (%)	1.15	1.65
$R_{DS(ON)}$ Temp. coefficient (175°C/25°C) (%)	1.45	2.64

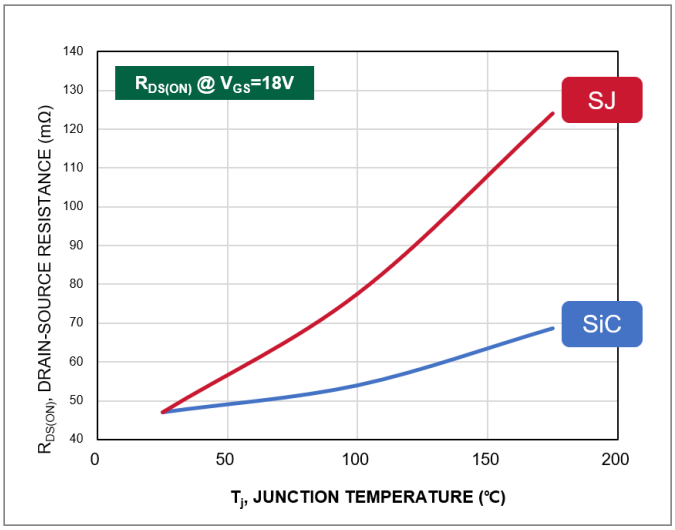
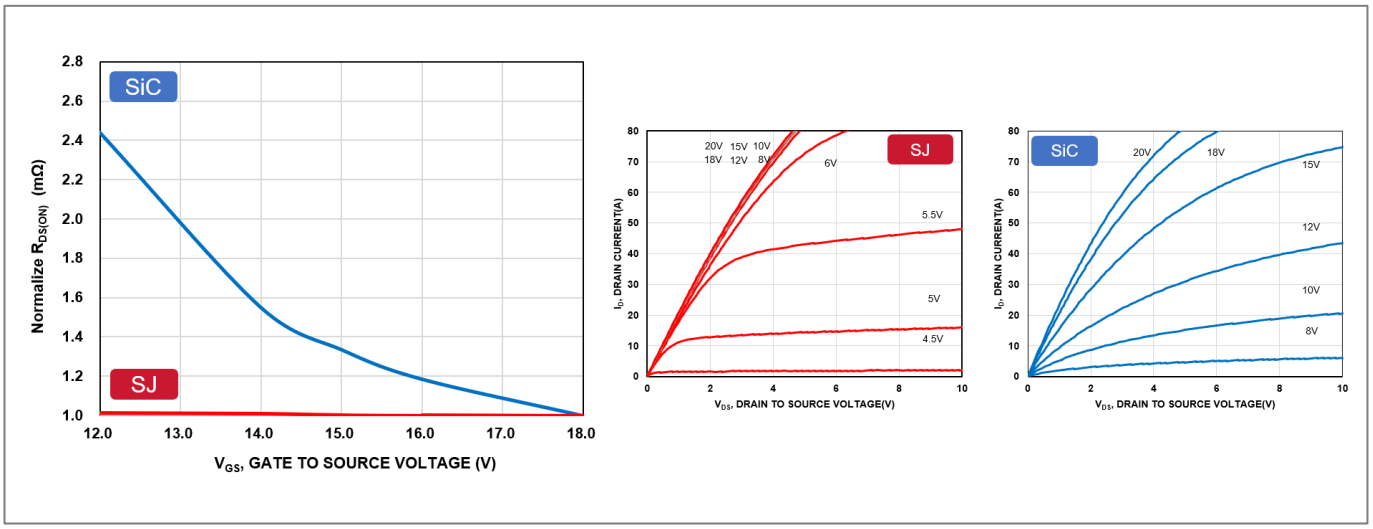


Figure 3. On-Resistance Characteristics Comparison vs. Temperature between Super-junction MOSFET and SiC MOSFET

The SiC MOSFET is different from a Super-junction MOSFET in that its on-resistance varies significantly depending on the operating V_{GS} value even when the channel is on. As shown in Fig. 4, $R_{DS(ON)}$ of SiC MOSFET is 2.4 times higher when it operates with 12V gate-source voltage but $R_{DS(ON)}$ of Super-junction is almost constant with gate-source voltage because a SiC MOSFET does not saturate at even 20V gate-source voltage, whereas a Super-junction MOSFET saturates at around 10V. Therefore, increasing the V_{GS} value is effective in fully delivering the performance of the SiC MOSFET by decreasing the on-resistance. It is also clear why 18V driving voltage is recommended for *e*SiC MOSFET M1 to maximize its performance. This does not mean that *e*SiC MOSFET M1 cannot be operated with lower gate-source voltage. Customers can select the driving voltage considering the required drain current, gate driving circuitry, temperature and efficiency while avoiding linear mode operation.

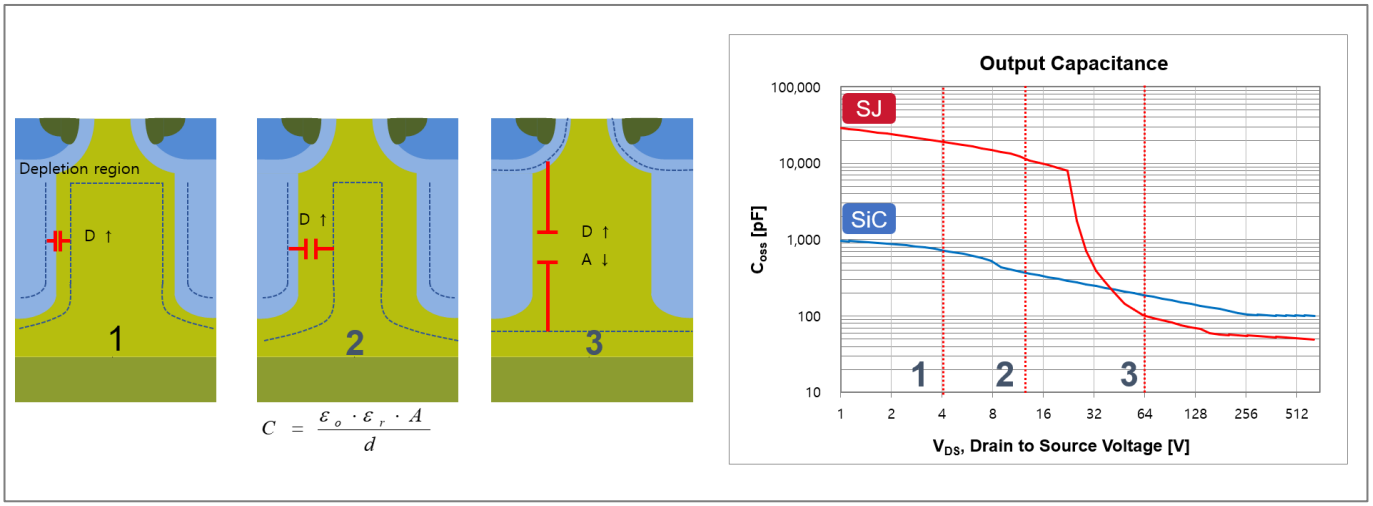


(a) Normalized $R_{DS(ON)}$ Comparison (b) On-Region Characteristics Comparison

Figure 4. Normalized $R_{DS(ON)}$ and On-Region Characteristics Comparison vs. V_{GS} between Super-junction MOSFET and SiC MOSFET

2.1.2. Output Capacitance : Coss

The depletion process of a Super-junction structure starts with lateral depletion, and Coss is linearly decreased at low drain-source voltage. After lateral depletion is complete, since there are no available ions in the pillars, vertical depletion occurs between the p+ region (p-body well) and the n+ region (drain) and Coss decreases very rapidly around 50V drain-source voltage [3]. However, the Coss of SiC MOSFET, which has a planar structure, shows moderately linear change as shown in Fig. 5.



(a) Depletion region of Super-junction MOSFET

(b) Coss Curve Comparison of Super-junction MOSFET and SiC MOSFET

Figure 5. Depletion region of Super-junction MOSFET and Coss Curve Comparison of Super-junction MOSFET and SiC MOSFET according to Drain-Source Voltage (V_{DS})

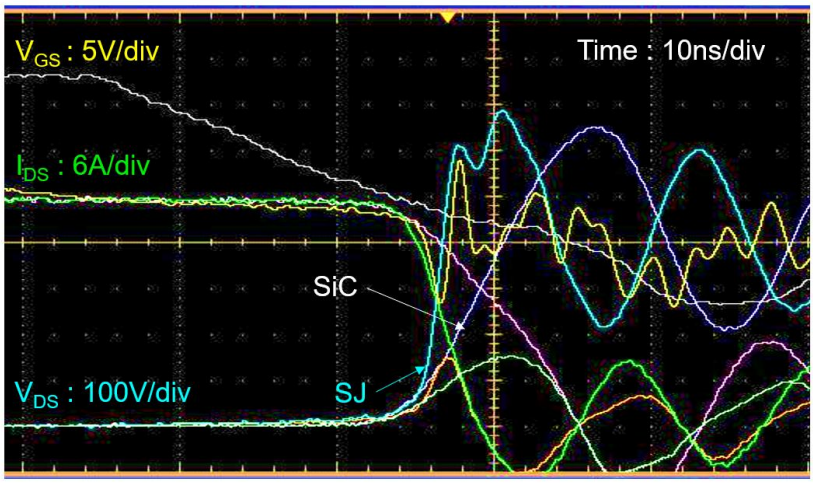
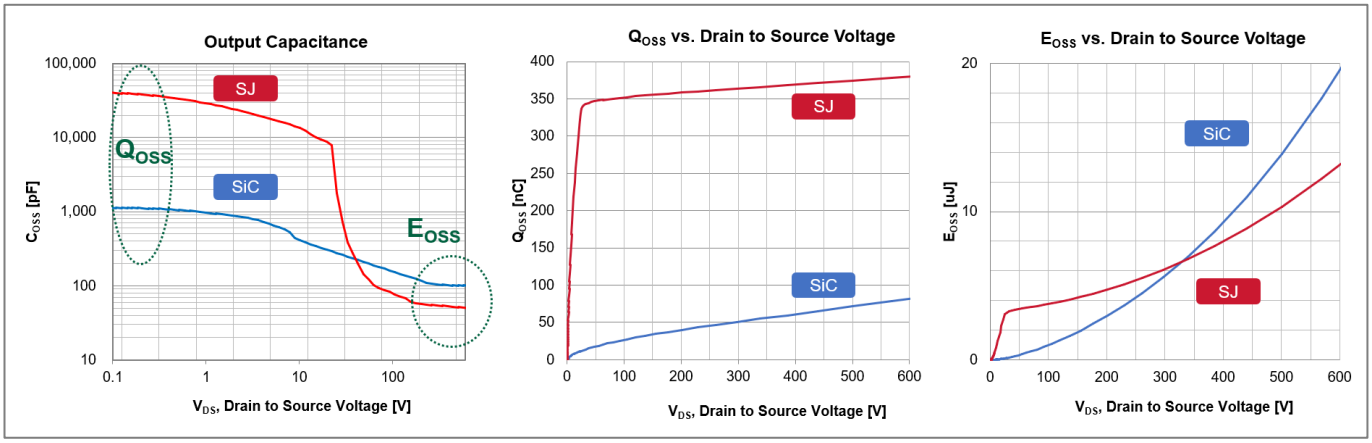


Figure 6. Comparison of Switching waveforms at Turn-off Transient of Super-junction MOSFET (color) and SiC MOSFET (white) under V_{DD}=400V, I_D=30A, R_G=4.7Ω, Free-wheeling Diode : SiC Diode

Strongly non-linear Coss behavior of Super-junction results in an extremely faster dv/dt and di/dt, causing higher voltage and current oscillation at turn-off transient compared to SiC MOSFET as shown in Fig. 6.

2.1.3. The charge on the output capacitance Q_{OSS} & The stored energy in the output capacitance, E_{OSS}



(a) C_{OSS} vs. V_{DS} (b) Q_{OSS} vs. V_{DS} (c) E_{OSS} vs. V_{DS}

Figure 7. C_{OSS}, Q_{OSS} and E_{OSS} Comparison of of Super-junction MOSFET and SiC MOSFET

Q_{OSS} is the amount of charge for charging drain-source capacity. Fig. 7 (b) shows Q_{oss} vs. Drain to Source Voltage. Q_{oss} is calculated as equation 1.

Equation 1) Q_{OSS}: The integral of the C_{OSS} along the drain to source voltage.

$$Q_{oss} = \int_0^{BV_{DSS}} C(v)\,\mathrm{dv}$$

C(v) is the capacitance by voltage as shown in Fig.25 (a)

As shown in Fig. 7 (b), Q_{OSS} value of Super-junction MOSFET at high voltage is determined by C_{OSS} at low voltage because Q_{OSS} is calculated the area under the C_{OSS} vs V_{DS} curve. The C_{OSS} value of Super-junction MOSFET shows a significant difference between high voltage and low voltage as explained in previous chapter. SiC MOSFET shows almost five times lower Q_{OSS} than that of Super-junction MOSFET at 400V due to its extremely low C_{OSS} at low voltage. The reduction in Q_{OSS} is critical to achieve zero-voltage switching (ZVS), the dead time between the high side and low side MOSFETs in the same leg must be long enough to allow the voltage transition. The dead time condition for achieving ZVS is given by equation 2.

Equation 2) Dead time condition for ZVS

$$\text{dead time} \geq 2 \cdot \frac{Qoss}{I}$$

where I is the current used to charge and discharge both FETs in the leg

Therefore, the maximum achievable switching frequency related to the charging and discharging transient of the drain to source is influenced by Q_{OSS}. As shown in Fig. 8, SiC MOSFET has a wider ZVS window than that of Super-junction MOSFET due to its faster switching transient of the high side and low side MOSFETs, enabled by lower Q_{OSS}. Therefore, SiC MOSFETs enable an increase in switching frequency, especially in resonant topologies.

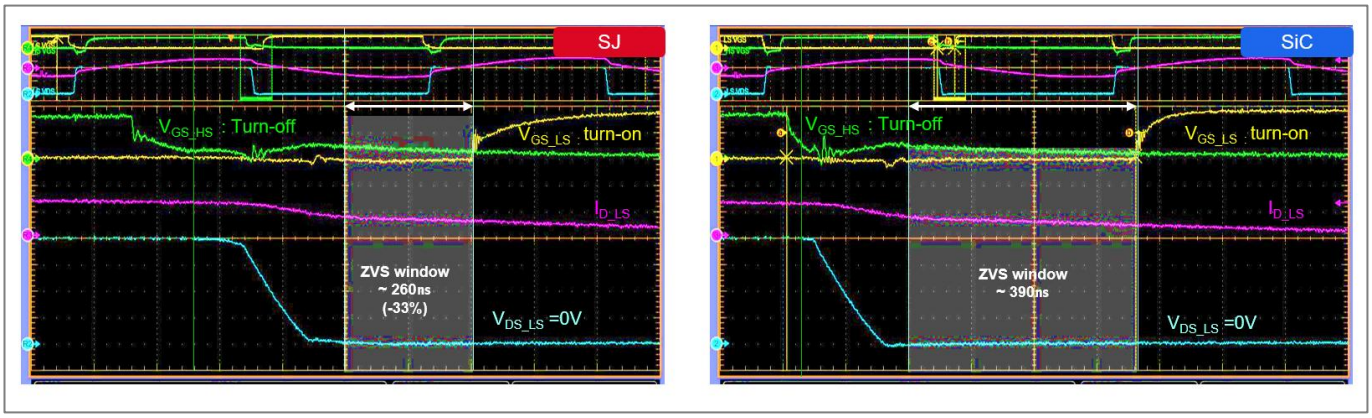


Figure 8. Comparison of ZVS Window Comparison at Switching Transient of Super-junction MOSFET and SiC MOSFET in LLC Resonant Converter.

The stored energy in the output capacitance (E_{OSS}) of a MOSFET can be calculated by integrating the product of the output capacitance and drain-source voltage with respect to the drain-source voltage from zero to the drain-source voltage just before the turn-on transient. E_{OSS} is calculated using equation 3.

Equation 3) E_{OSS}: The cumulated energy to output capacitor by the drain to source voltage

$$E_{oss} = \frac{1}{2}\left(C_{o(er)} \times {V_{DS}}^2 \right) = \int_0^{V_{DS}} C(v) \times v dv$$

C(v) is the capacitance by voltage as shown in Fig. 7.(a)

As shown in Fig. 7 (c), the E_{OSS} value of a Super-junction MOSFET at high voltage is more dependent on C_{OSS} at high voltage, because E_{OSS} is calculated by drain to source voltage multiplied by output capacitance or integral of the Q_{OSS} vs. V_{DS} graph in Fig. 7(b). Furthermore, the C_{OSS} value of a SiC MOSFET is higher than that of a Super-junction MOSFET at high voltage because of the 10 times thinner drift region of SiC MOSFET. Super-junction MOSFET shows lower E_{OSS} than the SiC MOSFET above 340V due to its extremely low C_{OSS} at high voltage.

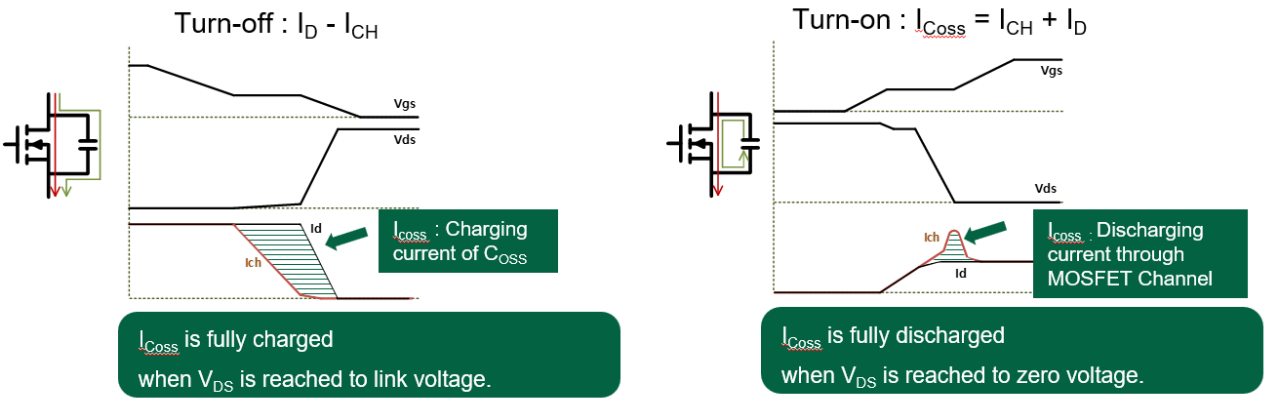


Figure 9. E_{OSS} dissipation Mechanism in during Turn-off and Turn-on transient in hard switching topology

Figure 9. clearly shows that the channel current (I_{ch}) is significantly lower than the drain current (I_D) during turn-off because drain current is diverted from the MOSFET channel to charge the output capacitor.

During the turn-on transient, The MOSFET channel conducts a significantly higher current than the drain current (I_d) because of the additional current coming from the discharging of the output capacitor. The stored energy in the output capacitance of the power MOSFET during turn-off is internally dissipated through the MOSFET channel in the form of Joule heating during turn-on in hard switching topology. This stored energy is dissipated through the channel of the MOSFET during every turn-on of the switching cycle. E_{OSS} of the MOSFET, is critical in hard-switching applications, such as flyback/forward converters or Power Factor Correction (PFC), especially at light loads and high switching frequencies, because it is fixed and independent of load.

2.1.4. Body Diode Performance Comparison

2.1.4.1. Body Diode Reverse Recovery Characteristics: Q_{RR}

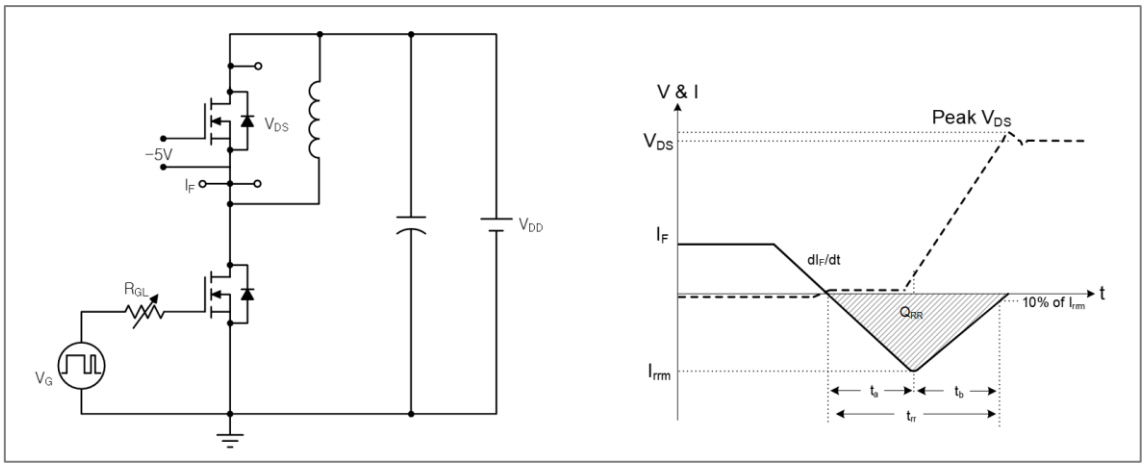
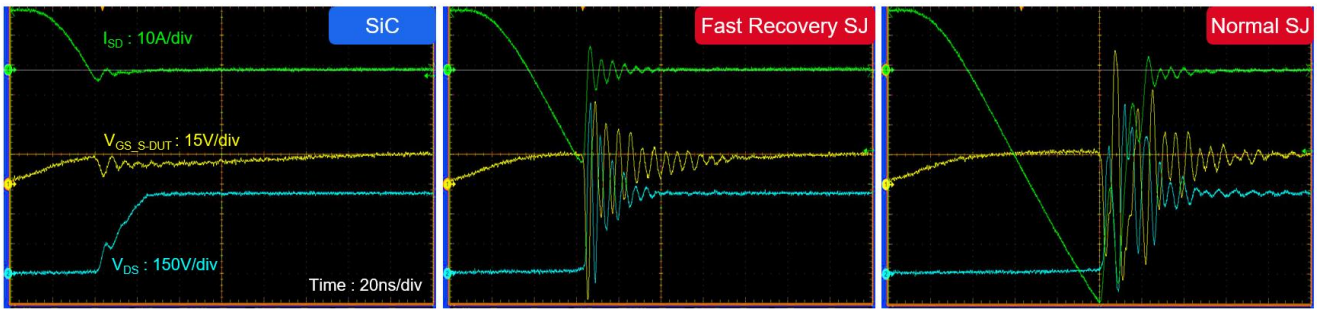


Figure 10. Body Diode Reverse Recovery Test Circuit and Waveforms.

The switching process of the diode from the on state to the reverse blocking state is called reverse recovery Fig. 10 shows reverse recovery test circuit and waveforms of MOSFET body diode. Firstly, the body diode conducts forward current for a while. During this period, charges are stored in the P-N junction of the diode. When reverse voltage is applied across the diode, stored charge must be removed to return to blocking state. The removal of the stored charge occurs via two phenomena: the flow of a large reverse current and recombination. A large reverse recovery current occurs in the diode during this process. [4].



(a) SiC MOSFET (b) Fast Recovery SJ MOSFET (c) Normal SJ MOSFET

Figure 11. Reverse recovery waveforms Comparison: Super-junction MOSFETs (Normal & Fast Recovery) and SiC MOSFET under V_{DD}=400V, I_{SD}=20A, V_{GS}=-3/+18V, di/dt=500A/μs and T_C=25°C

This reverse recovery current flows through the body diode of MOSFET because the channel is already closed. Some of the reverse recovery current flows right underneath N+ source. Body diode reverse recovery performance is very important for bridge topologies such as CCM totem-pole PFC or LLC resonant topologies for both system reliability and efficiency. Fig. 11 shows a reverse recovery waveforms comparison between Super-junction MOSFETs (normal & fast recovery) and SiC MOSFET under V_{DD}=400V, I_{SD}=20A, V_{GS}=-3/+18V, di/dt=500A/μs and T_C=25°C. The reverse recovery of the Super-junction MOSFET is very snappy because of extremely non-linear C_{OSS} by lateral and vertical depletion in deep p-type pillar-like structure. As shown in Fig. 11 (c), a snappy reverse recovery of the Super-junction MOSFET generates not only higher voltage spikes and drain voltage slew rates (dV_{DS}/dt) of high side MOSFET (DUT) but severe gate oscillation of low side MOSFET (S-DUT), which often results in device failure. Fast recovery Super-junction MOSFET has improved body diode performance by carrier lifetime control to reduce reverse recovery charge. As the reverse recovery charge (Q_{RR}) has reduced it results in much smaller peak reverse current (I_{RRM}) and less possibility to trigger parasitic BJT as shown Fig. 11 (b). Therefore, Fast recovery Super-junction MOSFET with improved body diode can provide higher ruggedness and better system reliability in for resonant topologies. Due to the improved body diode characteristics of the fast recovery Super-junction MOSFET, voltage spikes and gate oscillations have greatly reduced compared to normal Super-junction MOSFET. However, due to the snappy reverse recovery characteristics inherent in the Super-junction MOSFET structure, the dV_{DS}/dt of the drain voltage spike of high side MOSFET (DUT) and gate oscillation of low side MOSFET (S-DUT) is still high. In contrast, SiC MOSFET's planar structure not only possesses extremely soft reverse recovery behavior but results in lower Q_{RR} compared to fast recovery Super-junction MOSFET as shown in Fig 11 (a). This results in very low dV_{DS}/dt, of the drain voltage and minimized gate oscillation. As shown in Table 2, the reverse recovery charge (Q_{RR}) of fast recovery Super-junction MOSFET is 86% lower than that of normal Super-junction MOSFET and SiC MOSFET has 92% lower reverse recovery charge (Q_{RR}) than fast recovery Super-junction MOSFET Therefore, SiC MOSFETs are highly optimized switch solution for both resonant topologies and CCM totem-pole PFC topology that has hard commutation on body diode thanks to excellent body diode performance.

Table 2. T_{RR}, and Q_{RR}: Body Diode Performance Comparison: Super-junction MOSFETs (Normal & Fast Recovery) and SiC MOSFET.

DUT	SiC MOSFET	Fast Recovery Super-junction MOSFET	Normal Super-junction MOSFET
T_{RR} [ns]	18	71	211
Q_{RR} [μC]	0.09	1.17	8.44

2.1.4.2. Body Diode Forward Voltage: V_{SD}

One drawback of SiC MOSFET's body diode is its higher forward voltage drop (V_{SD}), compared to a Super-junction MOSFET because SiC has a wider band gap and thinner depletion region, which makes SiC MOSFET have poor minority carrier injection efficiency in the body SiC PN junction. This behavior is well-known for SiC MOSFETs in the third quadrant. Unlike a Si MOSFET, the SiC MOSFET's gate-channel is not completely closed at V_{GS} = 0 V, allowing partial current conduction. As a result, the voltage drop at V_{GS} = 0 V will be lower than for a negative value of V_{GS} as shown in Fig. 12. In other words, turn-off gate voltage strongly affects the body diode's forward voltage drop of SiC MOSFET as shown in Fig. 13. Therefore, understanding the third-quadrant characteristics of SiC MOSFETs is very important for designing and developing power conversion system that involve both forward and reverse current flow, such as motor drives, totem-pole PFCs and LLC resonant converters. High V_{SD} of SiC is significantly impacts efficiency in Totem-pole PFC or LLC resonant converters due to higher body diode conduction losses. An effective method to improve efficiency is to activate the MOSFET's channel, called synchronous rectification mode when reverse conduction is required or to reduce dead time to minimize reverse conduction through the body diode of SiC MOSFET.

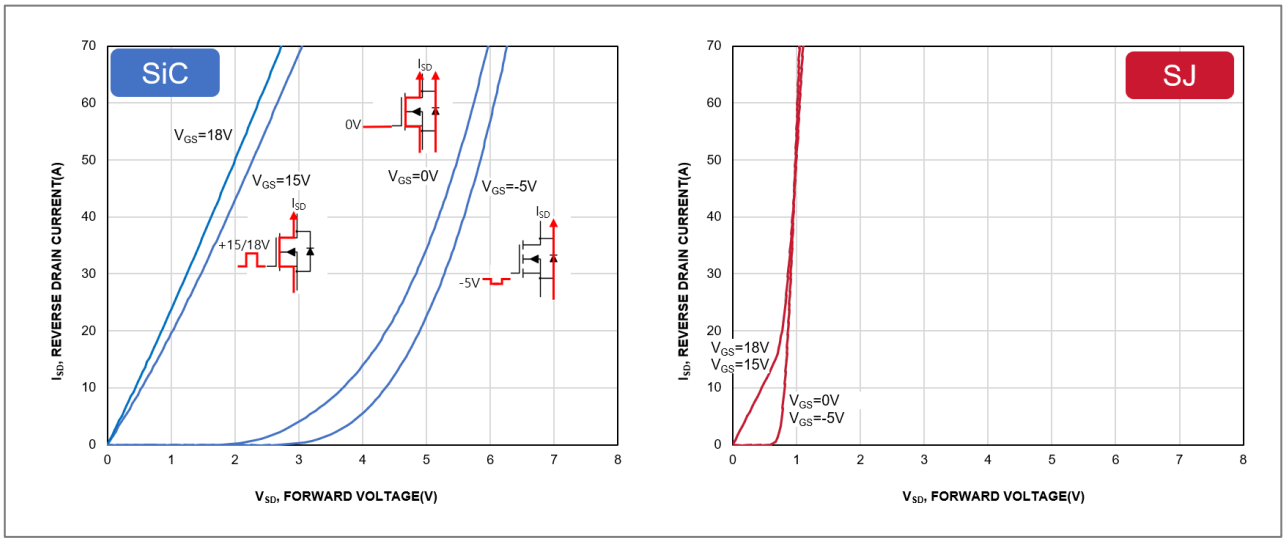


Figure 12. Body Diode Forward Voltage Characteristics vs. Source-Drain Current at Different Gate Voltage and TJ = 25℃

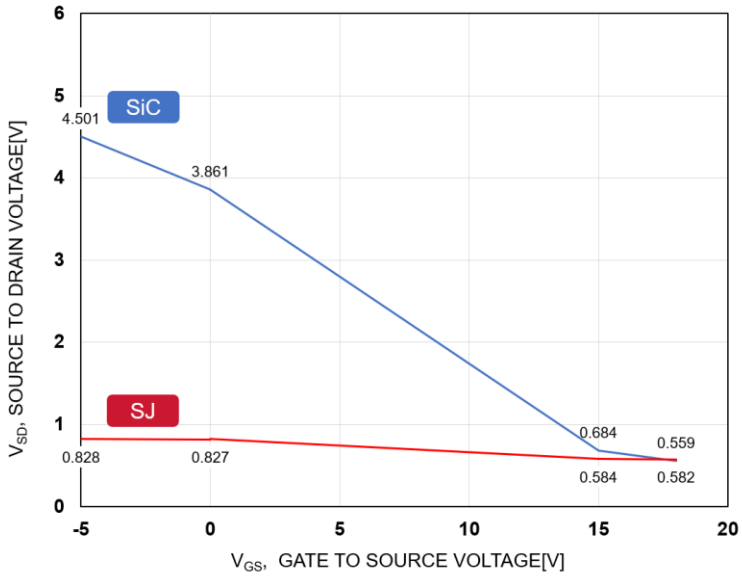


Figure 13. Body Diode Forward Voltage (V_{SD}) vs. Gate Voltage (V_{GS}) at TJ = 25℃

As shown in Fig. 14, synchronous rectification mode is highly recommended for reverse conduction operation to reduce body diode conduction losses. The voltage drop at positive bias is much lower than for that at zero or negative bias. Similar to the forward direction operation of the SiC MOSFET, the voltage drop in reverse direction mode with positive gate bias exhibits a positive temperature coefficient (PTC) characteristic, whereas it shows a negative temperature coefficient (NTC) characteristic with zero or negative gate bias as shown in Fig. 14.

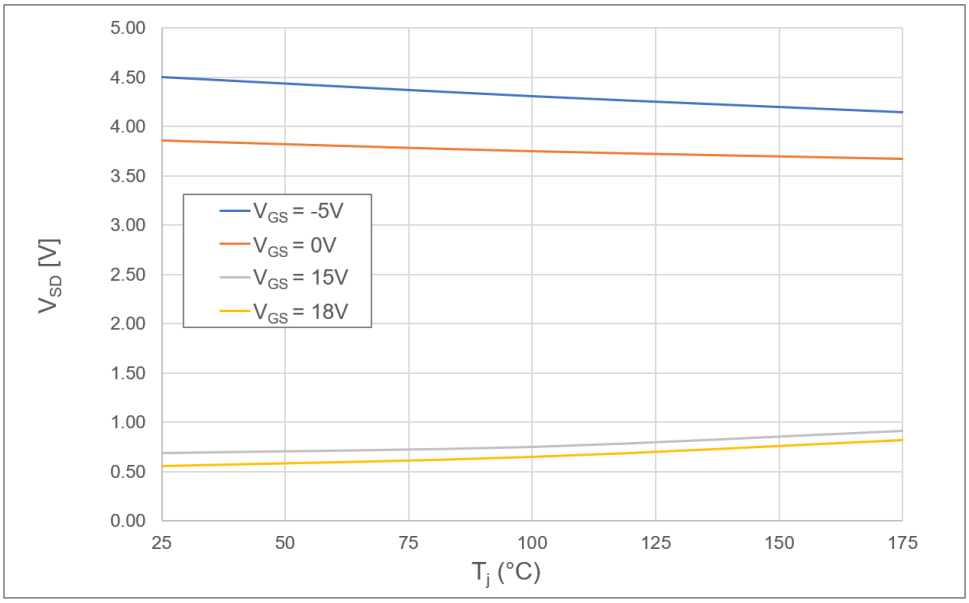


Figure 14. Body Diode Forward Voltage (V_{SD}) vs Temperature at Different Gate Voltages (V_{GS}) of SiC MOSFET

2.1.4.3. Gate Source Voltage: V_{GS}

There are two specifications regarding the gate-source voltage (V_{GS}) for 650V *e*SiC MOSFET in the datasheet as shown in table 3. The oxide layer of SiC MOSFET is easily damaged by over voltage even very small power. The V_{GS} rating is the maximum static gate to source voltage (DC) value. The upper and lower limits of continuous V_{GS} are set up to +22 V and -10 V. In any circumstance, the gate-source voltage should not exceed the rated value in datasheet. The V_{GSop} rating is the recommended operation value for turn-on (+18V) and turn-off gate volage (-5V).

Table 3. Gate to Source Voltage Specification in Datasheet of 650V *e*SiC MOSFET M1 and 600V *e*MOS, Super-junction MOSFETs.

Absolute Maximum Ratings (T_C = 25℃ unless otherwise noted) SiC

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	650	V
V_{GS}	Gate to Source Voltage (DC)	-10 / +22	V
V_{GSop}	Recommended Operation Value	-5 / +18	V

Absolute Maximum Ratings (T_C = 25℃ unless otherwise noted) SJ

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	600	V
V_{GSS}	Gate to Source Voltage	±30	V

Many characteristics of SiC MOSFET such as on-resistance ($R_{DS(ON)}$), switching losses and body diode voltage drop (V_{SD}), are highly dependent on the operating V_{GS} value. Power Master Semiconductor recommends driving the SiC MOSFET in certain voltage range considering conduction loss, switching losses, voltage spikes and false turn-on in real application. Super-junction MOSFET's maximum V_{GS} is ±30V and is much higher than SiC MOSFET due to its

thicker gate oxide structure. Unlike SiC MOSFET, the actual gate oxide breakdown voltage of Super-junction MOSFET is higher than the rated value in the datasheet. The V_{GSOP} of Super-junction MOSFET is not specified in the datasheet. Typically, Super-junction is operated at V_{GS}=0V ~10 or 12V as shown in Fig. 15.

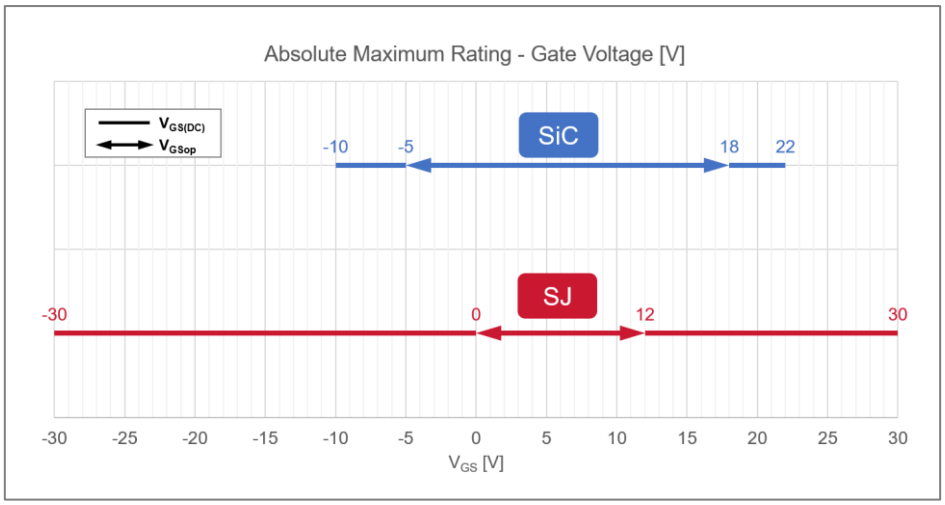


Figure 15. $V_{GS(DC)}$ and V_{GSop} Specification in Datasheet of SiC MOSFET. and Super-junction MOSFET

2.1.5. Dynamic Capacitive Loss E_{Dyn}: SiC MOSFET vs Super-junction MOSFET

The primary cause of dynamic capacitive loss by hysteresis anomaly is charge trapping due to the asymmetric depletion of the Super-junction columns, especially using a multi-epi process. During the charging, the depletion of the pn-junction progresses, leading to the formation of trapped holes within the center of the p-pillar. However, there are no electrons present on the n- epi during this phase. On the contrary, alternating holes and electron pockets are observed during the discharging. The pocket charges exit through a narrow path from the center of the pillar depletion region as a current. Fig. 16 shows simulated temperature profile of Super-junction MOSFET during charging (V_{DS}=0~400V) and discharging (V_{DS}=400~0V). Fig. 16 clearly shows trapped charges in specific charging pocket generated heat and power losses, and temperature is increased in charge pockets. This dynamic C_{OSS} loss is highly dependent on the switching frequency and operating drain-source voltage, dV/dt, and temperature. [5]

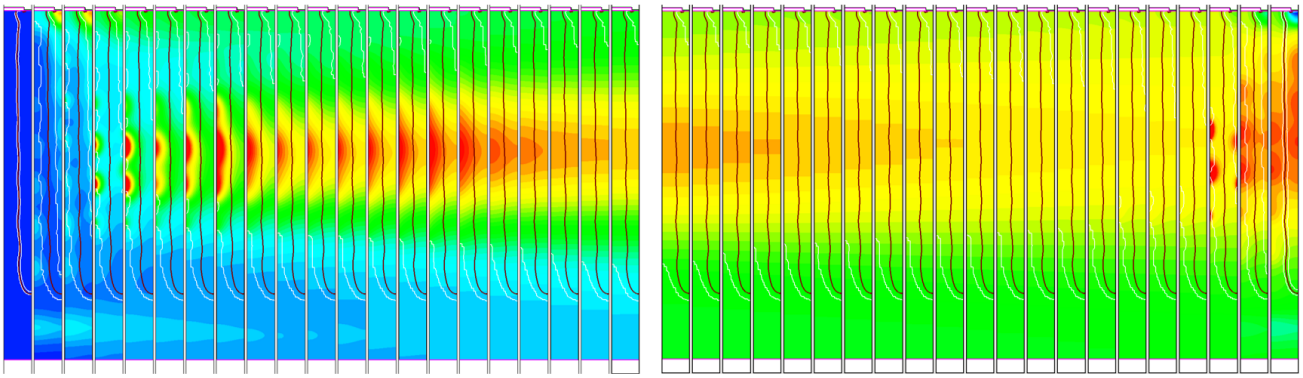


Figure 16. Simulated Temperature Profile of Super-junction MOSFET during Charging (V_{DS}=0~400V) and Discharging (V_{DS}=400~0V)

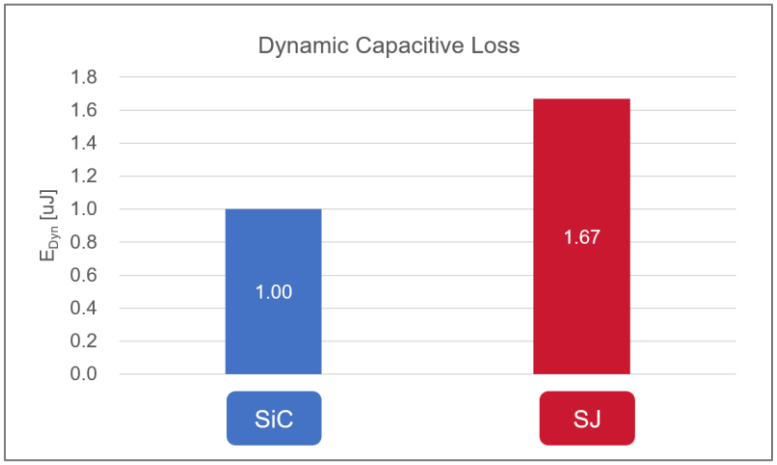


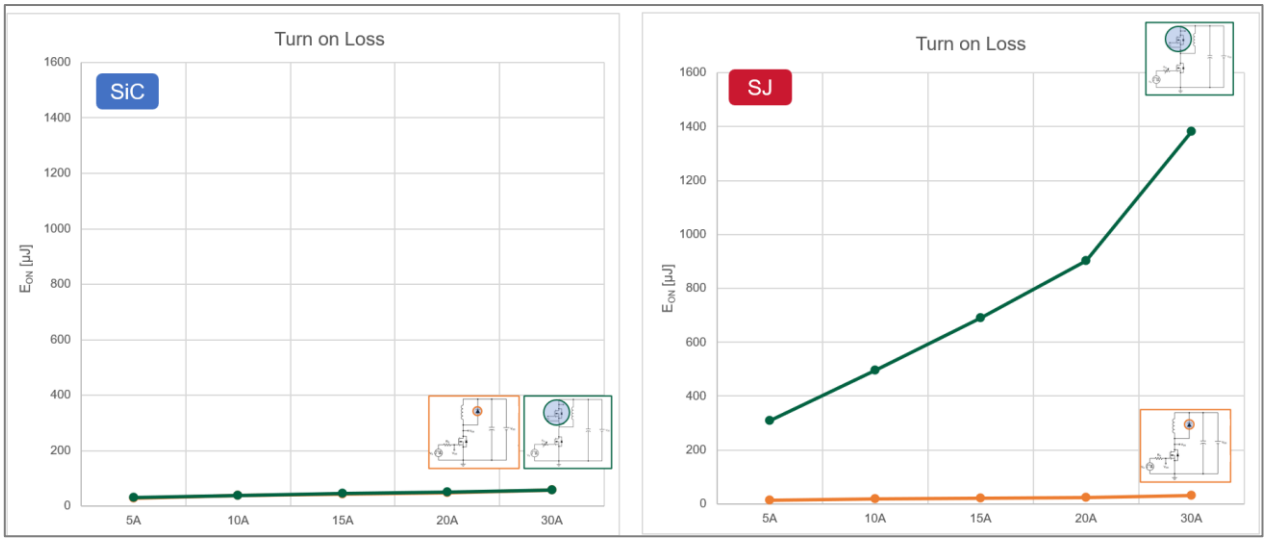
Figure 17. Normalized Dynamic C_{OSS} loss of SiC MOSFET vs. Super-junction MOSFET

Fig. 17 shows a normalized dynamic C_{OSS} loss of the Super-junction MOSFET and SiC MOSFET. The dynamic C_{OSS} loss of Super-junction MOSFET is 1.67 times higher than SiC MOSFET due to charge pocket by the asymmetric depletion and long p-pillar current path of the Super-junction MOSFET. Therefore, SiC MOSFET provides a significant efficiency advantage in high frequency operated soft switching topologies.

2.1.6. Switching Behavior Comparison: SiC MOSFET vs Super-junction MOSFET

2.1.6.1. Dependence of Switching Behavior on Freewheeling Diode

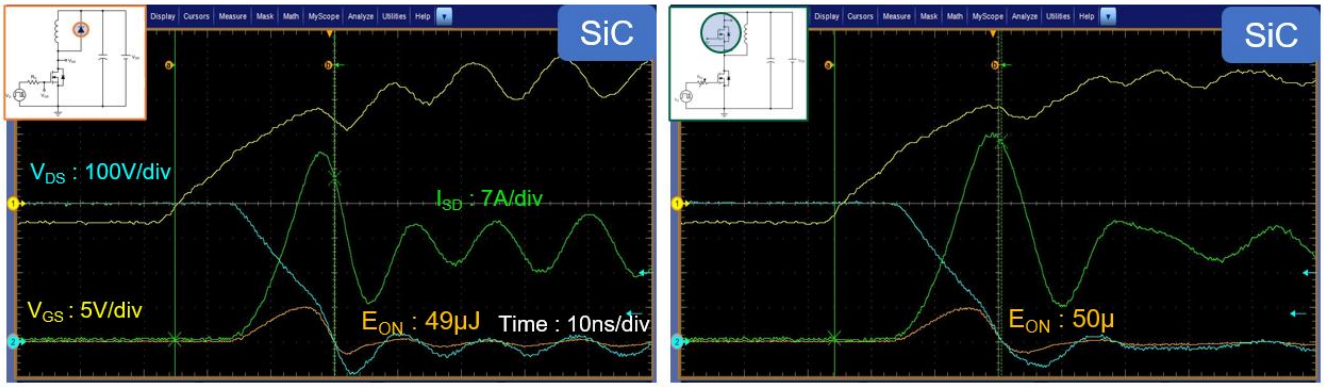
Unlike SiC MOSFET, switching losses of Super-junction MOSFETs are highly dependent on freewheeling diode due to the much larger reverse recovery charge (Q_{RR}) of body diode and output capacitance (C_{OSS}) than that of SiC MOSFET.



(a) SiC MOSFET (b) Super-junction MOSFET

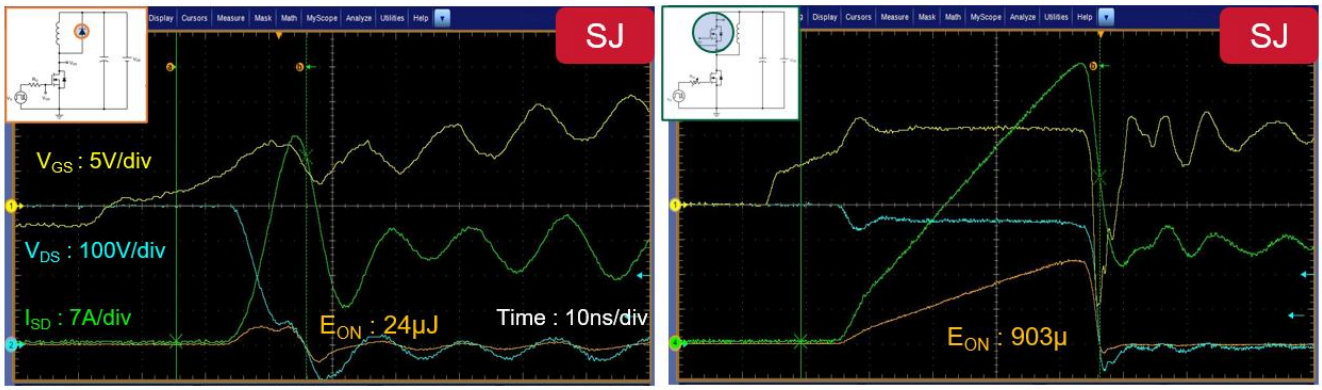
Figure 18. Turn-on Switching Losses Comparison of SiC MOSFET and Super-junction MOSFET according to Freewheeling Diodes: SiC diode (PCH65S16D1)(Orange) and Same DUT(Green) under V_{DD}=400V, I_D=5~30A, R_G=4.7Ω.

Fig. 18 shows the measured turn-on switching losses (E_{on}) compared between SiC MOSFET and Super-junction MOSFET with different free-wheeling diode, SiC diode (PCH65S16D1) (Orange) and same DUT(Green) under V_{DD}=400V, I_D=5~30A, R_G=4.7Ω. As shown in Fig. 18, SiC MOSFET shows similar turn-on losses regardless of the freewheeling diode. However, for Super-junction MOSFET, using the same DUT as the free-wheeling diode results in a significantly higher turn-on loss compared to using a SiC diode. Fig. 19 shows the turn-on switching waveforms of SiC MOSFET with different free-wheeling diode, SiC diode (PCH65S16D1) and same DUT under same condition. As shown in Fig. 19, SiC MOSFET shows similar turn-on waveforms according to freewheeling diode because Q_{RR} of SiC MOSFET's body diode is similar to that of SiC diode.



(a) Free-wheeling Diode: SiC Diode (b) Free-wheeling Diode: Body Diode of Same DUT

Figure 19. Turn-on Switching Waveforms of SiC MOSFET with Different Free-wheeling Diode: SiC Diode (PCH65S16D1) and Same DUT under V_{DD}=400V, I_D=5~30A, R_G=4.7Ω.

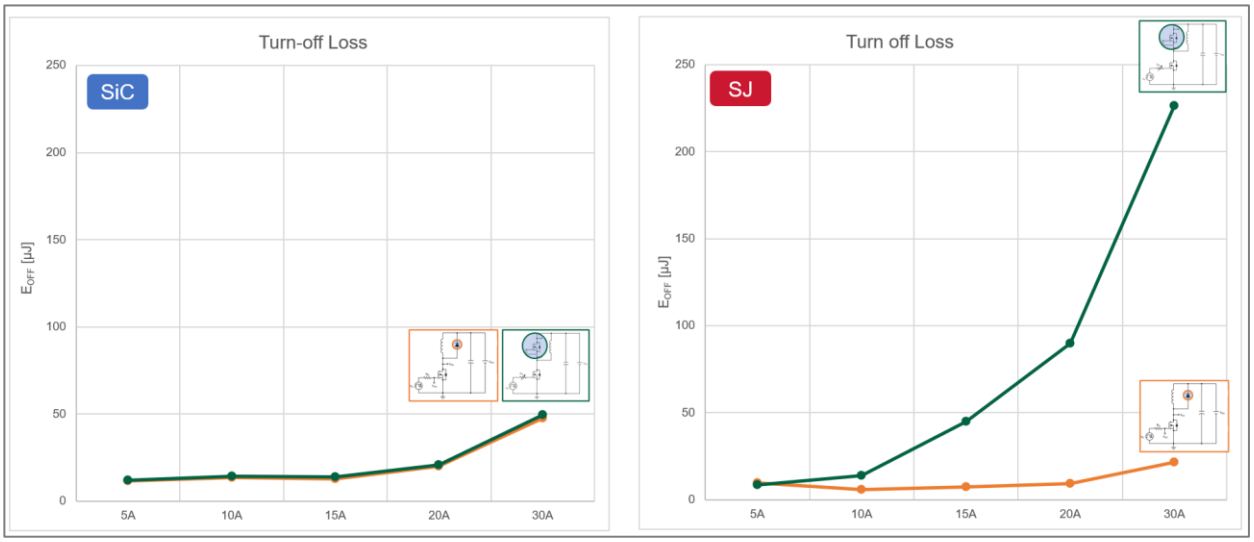


(a) Free-wheeling Diode: SiC Diode (b) Free-wheeling Diode : Body Diode of Same DUT

Figure 20. Turn-on Switching Waveforms of Super-junction MOSFET with Different Free-wheeling Diode: SiC Diode (PCH65S16D1) and Same DUT under V_{DD}=400V, I_D=5~30A, R_G=4.7Ω.

Fig. 20 shows the turn-on switching waveforms of Super-junction MOSFET with different free-wheeling diode, SiC diode (PCH65S16D1) and same DUT under same condition. For Super-junction MOSFET, employing the body diode as a free-wheeling diode results in a turn-on switching loss that is 37.5 times higher than that measured when using SiC diode as a free-wheeling diode. This is because the Q_{RR} of Super-junction MOSFET is significantly larger than

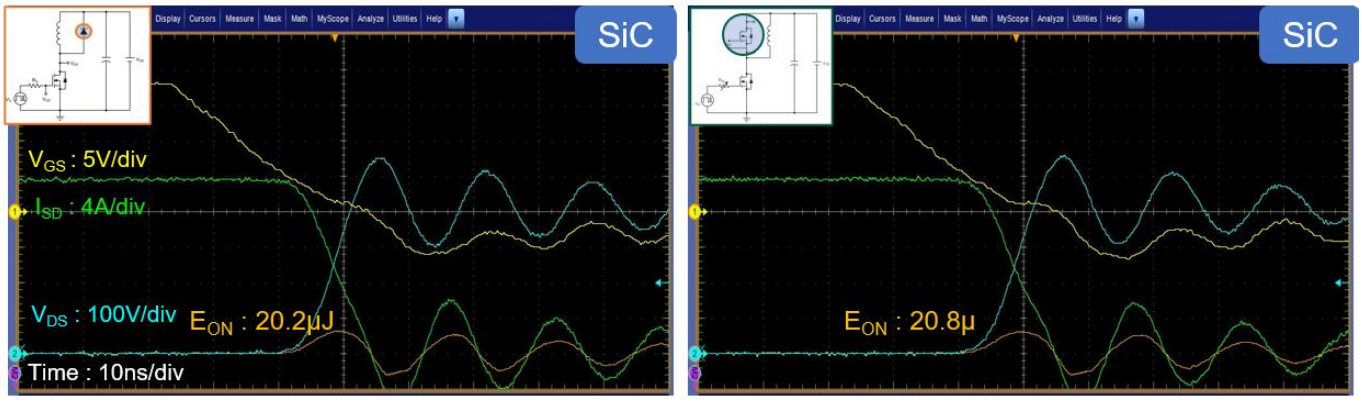
that of the SiC diode, and it has a significant impact on the turn-on switching loss.



(a) SiC MOSFET (b) Super-junction MOSFET

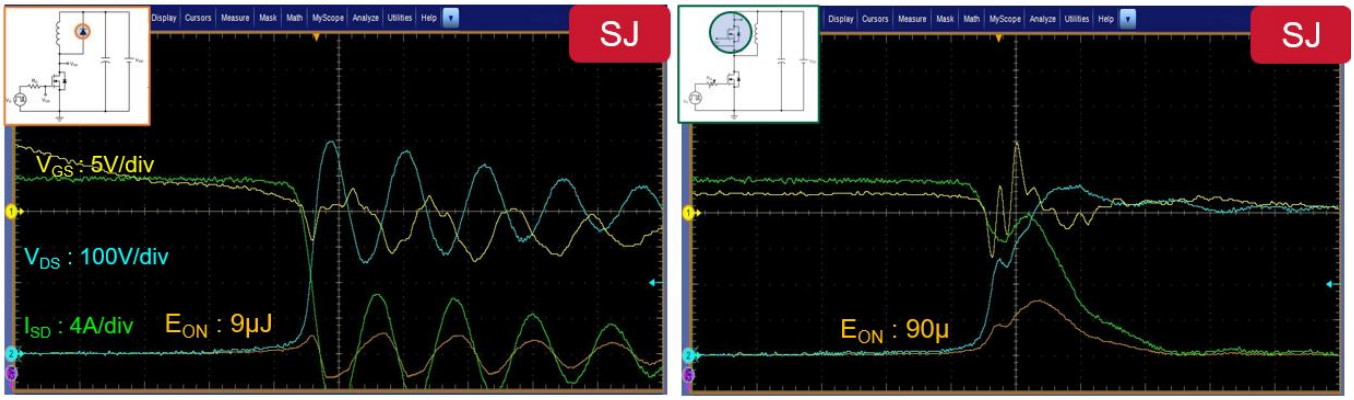
Figure 21. Turn-off Switching Losses Comparison of SiC MOSFET and Super-junction MOSFET According to Free-wheeling Diode: SiC Diode (PCH65S16D1) (Orange) and Same DUT (Green) under V_{DD}=400V, I_D=5~30A, R_G=4.7Ω.

Fig. 21 shows the measured turn-off switching losses (E_{off}) comparisons of SiC MOSFET and Super-junction MOSFET with different free-wheeling diode, SiC diode (PCH65S16D1) (Orange) and same DUT(Green) under V_{DD}=400V, I_D=5~30A, R_G=4.7Ω. As shown in Fig. 21, SiC MOSFET shows similar turn-off losses according to freewheeling diode. However, for Super-junction MOSFET, using the same DUT as the free-wheeling diode results in a significantly higher turn-off loss compared to using a SiC diode. Fig. 22 shows the turn-off switching waveforms of SiC MOSFET with different free-wheeling diode, SiC diode (PCH65S16D1) and same DUT under same condition. As shown in Fig. 22, SiC MOSFET shows similar turn-off losses according to freewheeling diode because C_{OSS} of SiC MOSFET is similar to junction capacitance of SiC diode.



(b) Free-wheeling Diode: SiC Diode (b) Free-wheeling Diode : Body Diode of Same DUT

Figure 22. Turn-off Switching Waveforms of SiC MOSFET with different freewheeling diode under V_{DD}=400V, I_D=5~30A, R_G=4.7Ω, Free-wheeling Diode: SiC Diode (PCH65S16D1)(Orange) and Same DUT(Green).



(b) Free-wheeling Diode: SiC Diode (b) Free-wheeling Diode : Body Diode of Same DUT

Figure 23. Turn-off Switching Waveforms of Super-junction MOSFET with different freewheeling diode under V_{DD}=400V, I_D=5~30A, R_G=4.7Ω, Free-wheeling Diode: SiC Diode (PCH65S16D1)(Orange) and Same DUT(Green).

Fig. 23 shows the turn-off switching waveforms of Super-junction MOSFET with different free-wheeling diode, SiC diode (PCH65S16D1) and same DUT under same condition. For Super-junction MOSFET, employing the same DUT as a free-wheeling diode results in a turn-on switching loss that is 10 times higher than that measured when using SiC diode as a free-wheeling diode. This is because the C_{OSS} of Super-junction MOSFET is extremely higher than junction capacitance of the SiC diode, and it has a significant impact on the turn-off switching loss. Strongly non-linear C_{OSS} of Super-junction MOSFET results in a re-turn-on phenomenon by higher gate voltage oscillation during turn-off transient. Therefore, Super-junction MOSFET is a good solution for classic boost PFC using SiC diode, but it cannot be used in fast leg of CCM totem-pole PFC due to its extremely high reverse recovery losses by poor body diode performance. SiC MOSFET is a highly optimized solution especially for bridge type topologies such as CCM totem-pole PFC and half-bridge or full bridge inverters, because SiC MOSFET offer extremely low switching energy loss by smaller reverse recovery charge and low conduction loss by lower temperature dependency of $R_{DS(ON)}$.

3. Target Applications of SiC MOSFETs and Si Super-Junction MOSFETs

Fig. 24 shows the target applications of SiC MOSFETs and Super-junction MOSFETs. The Super-junction MOSFETs are improved and proven technology for many applications over several decades. However, SiC MOSFETs offer many performance benefits such as higher breakdown voltage, lower switching losses, and lower $R_{DS(ON)}$ for surpass those of Super-junction MOSFETs. SiC MOSFETs enable higher switching frequencies and reduce passive component size, leading to high power density. However, SiC material remains more costly compared to Si material. The positioning of SiC MOSFET and Super-junction MOSFET is clear from a high-level perspective. Super-junction MOSFETs are more suitable for consumer and low power applications and SiC MOSFETs excel in applications requiring a combination of high temperature, high power, high voltage and high switching frequencies, offering significant performance improvements for the solar inverters, energy storage systems, main traction inverters, on-board chargers, DC EV chargers and AI datacenter power supplies.

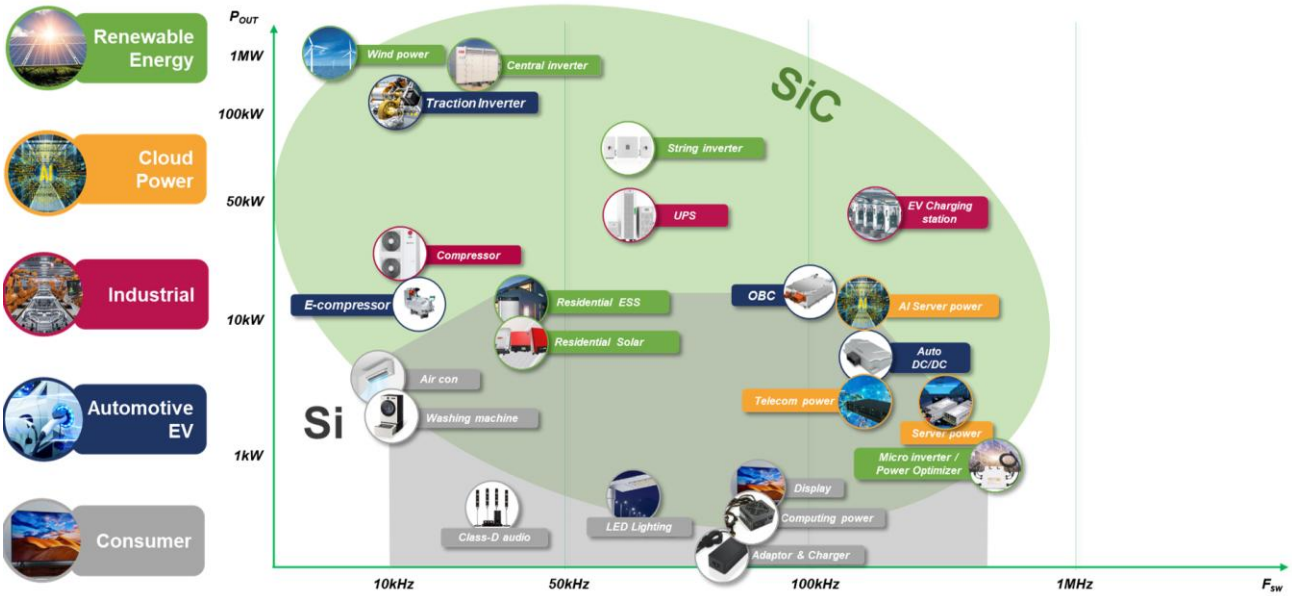


Figure 24. Target Applications of SiC MOSFETs and Super-junction MOSFETs

4. Summary

4.1.1. Required key parameters for each topology

Required key parameters of convention boost PFC

- Low FOM : $R_{DS(ON)}$ * Q_G
- Low E_{OSS} for higher light load efficiency.
- Low switching losses.
- Reasonable V_{DS} overshoot and gate oscillation.

Required key parameters of FAST leg switch for Totem-pole PFC

- Low FOM : $R_{DS(ON)}$ * Q_G for higher heavy load efficiency.
- Low E_{OSS} for higher light load efficiency.
- Low Q_{RR} of body diode for lower turn-on loss.
- Low V_{SD} of body diode.
- Low switching losses.
- Reasonable V_{DS} overshoot and gate oscillation.

Required key parameters of primary side switch for LLC resonant converter

- Conduction losses, which are dominated by $R_{DS(ON)}$ and its temperature coefficient.
- Low dynamic C_{OSS} (E_{DYN}) Loss for higher efficiency in light load.
- Soft reverse recovery and ruggedness of body diode for better system reliability under abnormal conditions.
- Small Q_{OSS} for short dead-time to minimize duty loss.

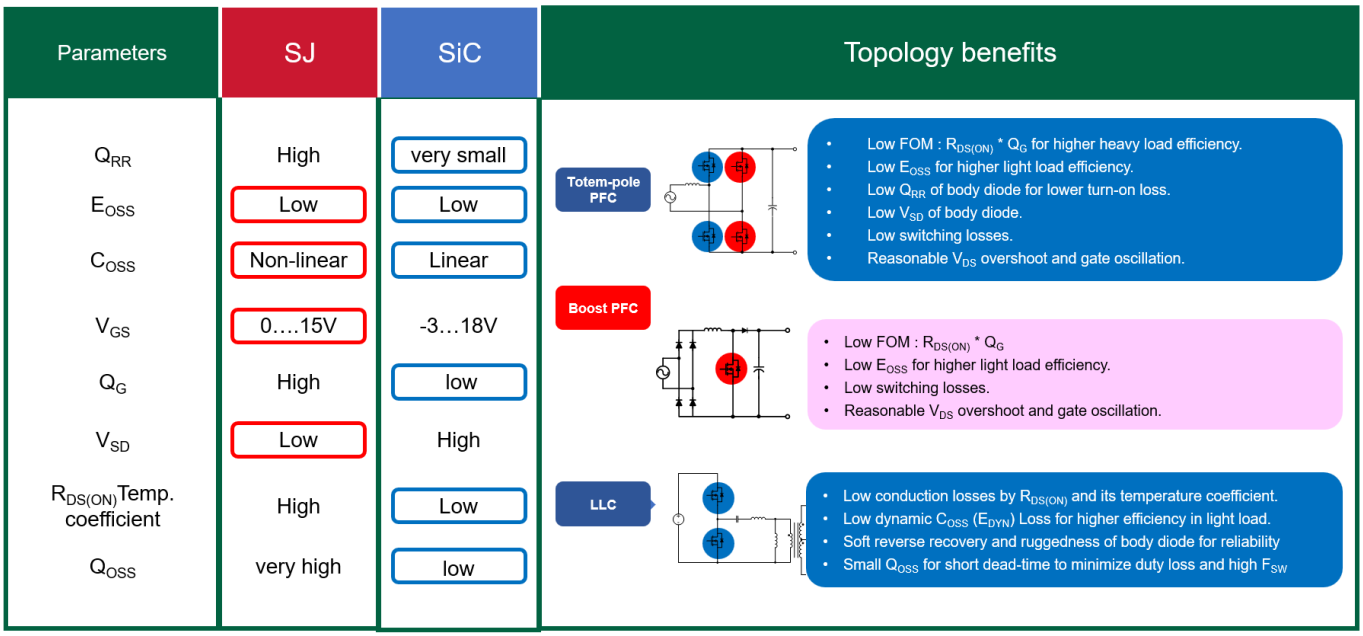


Figure 25. Key Characteristics and Topology Benefits of SJ MOSFETs and SiC MOSFETs

Totem-pole PFC

Each topology has its own specific requirements, therefore understanding the key characteristics of different semiconductor materials and technologies, adaption to different topologies, and the needs of each application can help in making decisions. Fig. 25 shows key characteristics and topology benefits of Super-junction MOSFETs and SiC MOSFETs. In CCM totem-pole PFC topology that has hard commutation on body diode, it is important to consider reverse recovery charge, Q_{RR} to reduce turn-on switching loss. SiC MOSFETs can reduce Q_{RR} by a factor of 10 compared to fast recovery Super-junction MOSFET. SiC MOSFETs are the right solution for higher efficiency in CCM totem-pole PFC. But Super-junction MOSFET can be used in line frequency operation leg.

Conventional boost PFC

In hard switching topology, the stored energy in C_{OSS} must be dissipated and EOSS of MOSFET is very critical in hard-switching applications such as flyback / forward converters or boost PFC, especially at light loads and high switching frequency, because it is fixed and independent of load. E_{OSS} of Super-junction MOSFET is still competitive against SiC MOSFET. Although Super-junction MOSFET exhibit lower output capacitance than SiC MOSFETs at a 50V drain-source voltage, and their C_{OSS}/V_{DS} relationship is significantly more non-linear. As a result, turn-off switching loss of Super-junction MOSFET is lower than SiC MOSFET. SiC MOSFET requires -3~18V to maximize performance in both $R_{DS(ON)}$ and switching losses. However, Super-junction MOSFET requires only 0~15V to driver for turn -on and turn-off, it doesn't require negative gate driving voltage for turn-off switching. Super-junction MOSFETs are the best choice as a cost-effective solution in conventional boost PFC.

LLC resonant converter

In resonant topologies that involve continuous hard commutation of the conducting body diode, it is crucial to consider the reverse recovery charge (Q_{RR}). This charge represents the amount that needs to be removed from the integrated body diode when the diode stops conducting. Thanks to the very low Q_{RR} of SiC MOSFETs, MOSFET failure can be avoided by body diode dv/dt during abnormal condition in LLC resonant converter. Compared to Super-junction MOSFET, the $R_{DS(ON)}$ of SiC MOSFETs is much more stable across a wide operating temperature range. The $R_{DS(ON)}$

of a SiC MOSFETs changes by only about 1.15 times between 25°C and 100°C, whereas a Super-junction MOSFET changes by 1.65 times under the same temperature range. This lower temperature dependency of $R_{DS(ON)}$ means that power loss is less affected by temperature, allowing SiC MOSFETs to operate efficiently at higher temperatures. SiC MOSFETs offer better system efficiency in LLC resonant converter. In another words, SiC MOSFETs are a suitable solution for high-temperature environments and often achieve the same efficiency with simpler cooling systems. Thanks to much lower Q_{OSS} of SiC MOSFETs, it is the right solution to increase switching frequency especially in LLC resonant topologies to reduce passive components. A drawback of SiC MOSFET is the higher forward voltage of body diode. SiC MOSFETs could lead to four times the conduction loss of body diode during dead time. Therefore, dead time must be optimized to maximize the benefits of SiC MOSFET in LLC resonant converters.

5. Conclusion

SiC MOSFETs offer significantly higher efficiency compared to Super-junction MOSFETs, but choosing the right technology often involves balancing various trade-offs. Although SiC MOSFETs have many advantages compared to Super-junction MOSFET, they also present challenges including higher V_{SD}, driving voltage and $V_{GS(th)}$ shift. It is crucial to understand the advantages and disadvantages of SiC and Super-junction devices. This application note described the key device factors for different topologies to help optimize design for better efficiency, reliability and cost-effectiveness in various applications.

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7. Document Revision History

Major changes since the last version

Date	Description of change
25-March-2025	First Release

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